REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed May 29, 2007. Claims 1-13 remain pending in the present application. The drawings were objected to for failing to comply with 37 CFR §1.121(d). Claims 1-13 were rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Priem et al.* (U.S. Pat. No. 6,282,587, hereinafter "*Priem*"), in view of *Radko* (U.S. Pat. No. 5,687,392), further in view of *Beshai et al.* (U.S. Pub. No. 2004/0213291, hereinafter "*Beshai*"), further in view of *Saito* (U.S. Pat. No. 6,198,746). Applicants respectfully request consideration of the following remarks contained herein. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

I. Objections to the Drawings

On page 2, the Office Action indicates that the drawings are objected to for failing to comply with 37 CFR 1.121(d) because some of the figures are not legible. The Office Action referenced and allegedly-attached "Notice of Draftsperson Patent Drawing Review" for details. However, no such notice was attached to the Office Action (indeed, the summary page of the Office Action indicates that only a Form PTO-892 was attached). Therefore, the Office Action has not properly advised Applicants of the informalities in the drawings that require correction. Furthermore, Applicants respectfully submit that any required changes to the drawings be held in abeyance until after an indication of allowance (so as to minimize any unnecessary costs on the Applicants).

II. Response to Claim Rejections Under 35 U.S.C. § 103

Claims 1-13 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Priem*, in view of *Radko*, further in view of *Beshai*, further in view of *Saito*. For at least the reasons set forth below, Applicants traverse these rejections.

Independent Claim 1

Applicants respectfully submit that independent claim 1 patently defines over *Priem*, in view of *Radko*, further in view of *Beshai* for at least the reason that the combination fails to disclose, teach or suggest certain features in claim 1.

Claim 1 recites (emphasis added):

> 1. A method for transferring network packet data stored in memory to an output device, the method comprising the steps of:
> concatenating one or more packet data octets from at least a first data word having at least one packet data octet to be included in a network packet to generate a first sequence of packet data octets having an octet length at least as great as an octet length of a data word;
> ***storing the first sequence of packet data octets in a FIFO buffer operably connected to the output device when the octet length of the sequence of packet data octets is equal to the octet length of a data word***; and
> ***storing a first subset of packet data octets from the first sequence of packet data octets in the FIFO buffer and storing a remaining second subset of packet data octets from the first sequence in an alignment register*** when the octet length of the first sequence of packet data octets exceeds the octet length of a data word, wherein an octet length of the first subset of packet data octets is equal to the octet length of a data word.

First, Applicants note that the Office Action addresses claims 1, 3, 5, 6, 7, 9, 10, 11, 12, and 13 collectively. (*See* Office Action, pages 4-6). However, while the Office Action addresses claim 1 (and apparently claim 5), the Office Action only addresses some of the elements in the remaining claims. (*See* Office Action, page 5, 3rd paragraph to page 2, 1st paragraph.) As such, Applicants respectfully submit that the

rejections put forth in the Office Action fail to address all the claimed features and limitations in these claims, making it difficult for the Applicants to adequately respond to the Office Action. Applicants refer to the MPEP, which states: "Where a claim is rejected for any reason relating to the merits thereof if should be 'rejected' and the ground of rejection fully and clearly stated." MPEP § 707.07(d). The Office Action fails to identify with particularity which portions of the cited references disclose Applicants' various claimed limitations.

Regarding claim 1, the Office Action relies on the *Priem*, *Radko* and *Beshai* references to reject claim 1. The Office Action alleges the following:

> "*Priem et al. clearly discloses . . . storing the first sequence of packet data octets in a FIFO buffer (fig. 1 (FIFO), column 2, lines 1-9) operably connected to the output device (fig. 1 (I/O drvice) [sic]) when the octet length of the sequence of packet data octets is equal to the octet length of a data word (fig. 5a (data length equals FIFO))*."

(Office Action, page 4). Applicants respectfully disagree. While *Priem* discloses a FIFO buffer and an I/O device, *Priem* does not appear to disclose the limitation, "storing the first sequence of packet data octets in a FIFO buffer . . . <u>when the octet length of the sequence of packet data octets is equal to the octet length of a data word</u>." In alleging that *Priem* teaches this limitation, the Office Action refers to FIG. 5A in the *Priem* reference. The related text for FIG. 5A is shown below (emphasis added):

> FIGS. 5A-5D illustrate formats of various commands which may be executed by a direct memory access controller designed in accordance with the present invention.

(BRIEF DESCRIPTION OF THE DRAWINGS).

> In general, the commands involve a number of methods for moving data. These commands are implemented in some circumstances by a "**<u>method count</u>**" (a move data command) which describes the

> operation, **an amount of data**, and an offset in the transfer buffer at which data resides which is to be transferred to an I/O device. In its simplest form (shown in FIG. 5A), **the command is indicated by "000" in the high order bits 29-31, the command includes a count which indicates the number of bytes of method data which are to follow**, indicates a DMA subchannel to be used for the transfer and an offset into the DMA engine. This is followed by a series of sequences of data each of which is offset sequentially in increments of one from the "get" offset in the transfer buffer. In implementing this command, the state machine causes the DMA engine to increment the offset at which data is read from the transfer buffer and increments the offset to which the data is written in the I/O control unit. This allows a long sequence of data to be transferred with a single command to a number of individual registers on the I/O control unit.

(Column 9, lines 39-58). While *Priem* teaches of commands implemented by a "method count" which describes, among other things, an amount of data, *Priem* fails to teach the element of "storing . . . when the octet length of the sequence of packet data octets is equal to the octet length of a data word." In referring to FIG. 5A in *Priem*, the Office Action only states "*data length equals FIFO.*" (Office Action, page 4). However, Applicants fail to understand how FIG. 5A (shown below) teaches storing . . . when the octet length of the sequence of packet data octets is equal to the octet length of a data word.

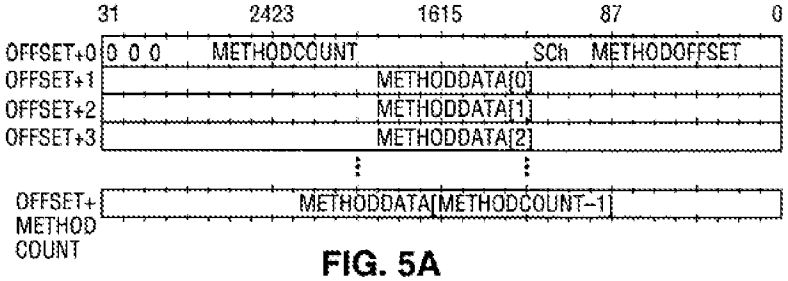

FIG. 5A

As such, Applicants respectfully submit that *Priem* fails to teach of "storing the first sequence of packet data octets in a FIFO buffer . . . when the octet length of the sequence of packet data octets is equal to the octet length of a data word."

Regarding the *Radko* reference, the Office Action maintains that "*Radko clearly discloses and shows an alignment register (fig. 3, dynamically allocated DMA transfer Buffer (387)) and the storing of packet sequence which is longer than the data word (column 7, lines 58-61)*." The cited text passage is shown below:

> Alternatively, when the evaluator 381 determines that the user buffer is of a suitable size for DMA block transfer, the dynamic allocator 383 dynamically allocates a DMA transfer buffer 387 (step 440). After dynamically allocating the DMA transfer buffer, the preferred embodiment determines when the user buffer conforms with the physical requirements of a DMA transfer buffer (step 450).

Applicants respectfully submit that while *Radko* teaches that the evaluator 381 determines that the user buffer is of a suitable size for DMA block transfer, *Radko* fails to teach of "storing a first subset of packet data octets from the first sequence of packet data octets in the FIFO buffer and storing a remaining second subset of packet data octets from the first sequence in an alignment register." Specifically, *Radko* fails to teach of storing a remaining second subset of packet data octets from the first sequence in the dynamically allocated DMA transfer buffer (387) (allegedly the "alignment register" recited in claim 1).

Accordingly, for at least the reasons above, Applicants respectfully submit that independent claim 1 patently defines over the cited references for at least the reason that the references fails to disclose, teach or suggest the highlighted features in claim 1 above.

Dependent Claims 2-4

Applicants submit that dependent claims 2-4 are allowable for at least the reason that these claims depend from an allowable independent claim. *See, e.g., In re Fine*, 837 F. 2d 1071 (Fed. Cir. 1988).

Independent Claim 5

Applicants respectfully submit that independent claim 5 patently defines over *Priem*, in view of *Radko*, further in view of *Beshai* for at least the reason that the combination fails to disclose, teach or suggest certain features in claim 5.

Claim 5 recites (emphasis added):

> 5. A system for transferring network packet data stored in memory to an output device, the system comprising:
> a direct memory access (DMA) interface for accessing a set of data words stored in memory, each data word having at least one valid octet to be included in a network packet and each data word being accessed using a DMA address associated with the data word;
> a first in-first out (FIFO) buffer for storing network packet data to be transmitted by the output device; and
> an alignment block having at least one alignment register, wherein the alignment register for storing at least one data octet, and wherein the alignment block is adapted to:
> concatenate one or more packet data octets from at least a first data word having at least one packet data octet to be included in a network packet to generate a first sequence of packet data octets having an octet length at least as great as an octet length of a data word;
> ***store the first sequence of packet data octets in a FIFO buffer operably connected to the output device when the octet length of the sequence of packet data octets is equal to the octet length of a data word***; and
> ***store a first subset of packet data octets from the first sequence of packet data octets in the FIFO buffer and storing a remaining second subset of packet data octets from the first sequence in an alignment register when the octet length of the first sequence of packet data octets exceeds the octet length***

of a data word, wherein an octet length of the first subset of packet data octets is equal to the octet length of a data word.

As noted earlier, the Office Action addresses claims 1, 3, 5, 6, 7, 9, 10, 11, 12, and 13 collectively and fails to point out with particularity which portions of the cited references disclose Applicants' various claimed limitations. The Office Action again appears to rely on the *Priem*, *Radko*, and *Beshai* references to reject claim 5. As discussed above, Applicants disagree and submit that the cited references fail to teach the elements, as alleged by the Office Action.

While *Priem* teaches of commands implemented by a "method count" which describes, among other things, an amount of data, *Priem* fails to teach the element, "store . . . when the octet length of the sequence of packet data octets is equal to the octet length of a data word." In referring to FIG. 5A in *Priem*, the Office Action only states "*data length equals FIFO.*" (Office Action, page 4). However, Applicants fail to understand how FIG. 5A teaches the feature emphasized in claim 5. Applicants respectfully submit that *Priem* fails to teach this feature.

Regarding the *Radko* reference, the Office Action maintains that "*Radko clearly discloses and shows an alignment register (fig. 3, dynamically allocated DMA transfer Buffer (387)) and the storing of packet sequence which is longer than the data word (column 7, lines 58-61)*." Applicants respectfully submit that while *Radko* teaches that the evaluator 381 determines that the user buffer is of a suitable size for DMA block transfer, *Radko* fails to teach the element, "store a first subset of packet data octets from the first sequence of packet data octets in the FIFO buffer and storing a remaining second subset of packet data octets from the first sequence in an alignment register." Specifically, *Radko* fails to teach of storing a remaining second subset of packet data

octets from the first sequence in the dynamically allocated DMA transfer buffer (387) (allegedly the "alignment register" recited in claim 5).

Accordingly, for at least the reasons above, Applicants respectfully submit that independent claim 5 patently defines over the cited references for at least the reason that the references fails to disclose, teach or suggest the highlighted features in claim 5 above.

Dependent Claims 6-13

Applicants submit that dependent claims 6-13 are allowable for at least the reason that these claims depend from an allowable independent claim. *See, e.g., In re Fine*, 837 F. 2d 1071 (Fed. Cir. 1988).

CONCLUSION

Applicants respectfully submit that all pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephone conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

No fee is believed to be due in connection with this response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 50-0835.

Respectfully submitted,

/Daniel R. McClure/

Daniel R. McClure
Reg. No. 38,962

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.
100 Galleria Parkway NW
Suite 1750
Atlanta, Georgia 30339
(770) 933-9500